Hybrid Imaging Technology
A Workable Approach to CCD/CMOS For Scientific Quality Imaging

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Recently work was begun at JPL to create a next-generation imager technology, called Hybrid Imaging Technology (HIT), that offers scientific quality performance. The key element of this technique is the merging of CCD and CMOS technologies by device hybridization rather than device fabrication. HIT offers the exceptional quantum efficiency, fill factor, broad spectral response, and very low noise properties of CCD imagers with the low power operation and flexibility of integration found in CMOS devices. charge-coupled device scientific imaging

The imaging portion of a HIT detector is identical to that found in a conventional CCD array. Charge is collected and held in a series of pixelated wells formed in an epitaxial silicon layer by electrically isolated, optically transparent, polysilicon control gates that overlay the imaging area. Collected charge is transferred in a pixel by pixel manner to the output structure by the application of a sequence of pulses to the control gates. However, unlike a CCD, the charge-to-voltage conversion in a HIT detector takes place in a charge-mode amplifier constructed in CMOS technology. This CMOS amplifier is bump-bonded to the main imaging portion of the array using standard technology.

Since the imaging portion of the HIT detector is simply a CCD, the resulting imager possesses all of the strengths of CCD technology, i.e., the HIT approach provides an inherent 100% optical fill factor and excellent quantum efficiency over a very broad spectral range (soft x-ray to near infrared). It also offers complete compatibility with backside thinning and illumination, including compatibility with JPLs patented Delta Doping backsurface pinning technology. These benefits are supported only by HIT (and its parent CCD) technology, and cannot be implemented in CID, APS, or any other CMOS-based device due to inherent architecture and CMOS process-related incompatibilities.

This hybrid approach allows both CCD and CMOS technologies to be independently optimized, providing the ultimate imaging performance in a highly miniaturized format. Hybridization also allows for reuse of imager arrays and CMOS readouts without the costly process of refabrication. A supply of unhybridized components can be maintained and appropriate combinations of components can be selected to match specific mission requirements.

Figure 1 is a photomicrograph of a prototype 256 x 512 element, 12 micron pixel, HIT array complete with a CMOS charge-mode amplifier. Figure 2 is a typical image from the array, with the brightest portion of the image corresponding to less than 1000 electrons. Noise data obtained from photon transfer curves indicate that the HIT array has an rms noise floor of 4.8 electrons at -30 C when operated at 25 kilopixels/sec. This is a promising start for the HIT technology. Future work will concentrate on reducing the noise floor and incorporating additional signal processing features into the CMOS component.

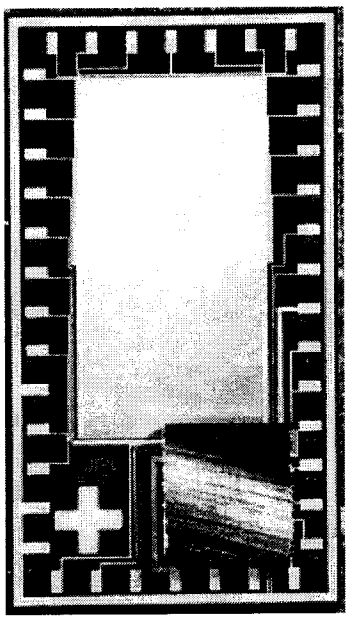

Figure 1. A 256 x 512 pixel HIT detector.

Figure 2. Image obtained from HIT device at 0 C with no background correction.